REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendment and the following remarks.

Summary of the Response

By the foregoing amendment, claims 44, 48, 52, 55 and 56 have been amended. Claims 1-43 have been canceled. Thus, claims 44-56 are currently pending in the application and subject to examination.

In the Office Action mailed on November 2, 2004, claims 44-51 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,970,009 to Hoenigschmid, et al. Claims 52-56 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hoenigschmid, et al. in view of U.S. Patent No. 6,445,932 to Soini, et al. To the extent that the rejections remain applicable to the claims currently pending, the Applicants hereby traverse the rejections, as follows.

Claim 44 Recites Patentable Subject Matter

Regarding claim 44, Applicants respectfully submit that Hoenigschmid, et al. fails to disclose or suggest at least the feature of "entering a low power consumption mode, in which the dynamic memory cells do not retain data therein by prohibiting refresh operations, in response to a dedicated external control signal supplied from an exterior via a dedicated external terminal in order to control the low power consumption mode," as recited in claim 44, as amended.

Hoenigschmid, et al. is directed to reducing standby current in a DRAM during standby mode. In Figure 4, Hoenigschmid, et al. discloses a monitor circuit 401 that detects whether the system is in standby or non-standby mode. If refresh is necessary,

the memory is in non-standby mode, and if refresh is not necessary, the memory is in standby mode. Whether refresh is necessary is determined by a CAS before RAS (CBR) signal and a RAS counter (RAScounter) signal. An active RAScounter signal indicates that no refresh activity has occurred within the predetermined time. *See* Hoenigschmid, et al., column 4, lines 33-44. Thus, Hoenigschmid, et al. only discloses that the CBR signal and the RAScounter signal for entering the semiconductor memory into a low power consumption mode are signals generated inside the semiconductor memory, and not control signals dedicated for controlling the low power consumption mode. *Id.* As a result, Hoenigschmid, et al. cannot achieve the effect of the present invention of having the "DRAM reliably enter the low power consumption mode and be released from the mode by the dedicated low power consumption mode signal /LP," as described, in connection with the preferred embodiment, on page 32, lines 15-17 of the specification of the present application.

Nothing in Hoenigschmid, et al., therefore, discloses or suggests the feature of the of "entering a low power consumption mode, in which the dynamic memory cells do not retain data therein by prohibiting refresh operations, in response to a dedicated external control signal supplied from an exterior via a dedicated external terminal in order to control the low power consumption mode," as recited in claim 44, as amended. For at least this reason, Applicants submit that claim 44 is allowable over the cited prior art.

Claim 48 Recites Patentable Subject Matter

Regarding claim 48, Applicants respectfully submit that Hoenigschmid, et al. fails to disclose or suggest at least the feature of "outputting a dedicated control signal to a dedicated external terminal in order to control a low power consumption mode made by the semiconductor memory so that the semiconductor memory enters a low power consumption mode, in which the dynamic memory cells do not retain data therein by prohibiting refresh operations," as recited in claim 48, as amended. Nothing in Hoenigschmid, et al. teaches or suggests a way to enter or exit a semiconductor memory to or from a low power consumption mode in response to a dedicated external control signal supplied directly from the exterior of the semiconductor memory via an external terminal, as required by this claim. For at least this reason, Applicants submit that claim 48 is allowable over the cited prior art.

Claims 45-47 and 49-51 Recite Patentable Subject Matter

Applicants respectfully submit that, as claims 44 and 48 are allowable, claims 45-47 and 49-51, each of which depends from allowable claims 44 or 48, are likewise allowable over the cited prior art.

Moreover, Applicants submit that nothing in Hoenigschmid, et al. teaches or suggests at least the feature of "the semiconductor memory enter[ing] the low power consumption mode in response to a voltage change of the dedicated external control signal from a first voltage to a second voltage," as recited in claim 45 and of "changing a voltage of the dedicated control signal from a first voltage to a second voltage when outputting the dedicated control signal," as recited in claim 49 of the present application.

The voltages of 1.75V and 1.0V that the Examiner points to in Hoenigschmid, et al. (Office Action, at page 3) are voltage differences between the n-well and the p-well, and do not represent changes in voltages of a control signal. *See*, Hoenigschmid, et al., column 3, lines 35-59. Specifically, the semiconductor memory in Hoenigschmid, et al. enters the low power consumption mode when the passenable signal changes to the active level in response to the CBR signal and the RAScounter signal. *Id.* at column 4, lines 45-52. The n-band voltage generator turns off at this point. *Id.* at column 4, lines 53-58. The voltage of the n-well also changes at this point, from 0.75V to 0V, thereby changing the voltage difference between n-well and p-well (which is -1.0V) from 1.75V to 1.0V. *Id.* at column 3, lines 52-55.

For at least these reasons, Applicants submit that claims 45-47 and 49-51 are allowable over the cited prior art.

Claims 52, 55 and 56 Recite Patentable Subject Matter

Regarding claims 52, 55 and 56, Applicants respectfully submit that neither Hoenigschmid, et al. nor Soini, et al., nor the combination thereof discloses or suggests at least the features of an "external control signal supplied from an exterior via a dedicated external terminal in order to control the low power consumption mode," as recited in amended claim 52, an "external terminal . . . dedicated for receiving a dedicated external control signal to control the low power consumption mode," as recited in amended claim 55, and a "data terminal . . . dedicated for receiving a dedicated external control signal to control the low power consumption mode," as recited in amended claim 56 of the present invention. It is respectfully submitted that the cited references, alone or in combination, fail to disclose a way to enter a

semiconductor memory to a low power consumption mode in response to a dedicated external control signal supplied directly from the exterior of the semiconductor memory via an external terminal, in order to control the low power consumption mode, as required by claims 52, 55 and 56 of the current invention.

For at least these reasons, Applicants submit that claims 52, 55 and 56, as amended, are allowable over the cited prior art.

Claims 53 and 54 Recite Patentable Subject Matter

Applicants respectfully submit that, as claim 52 is allowable, claims 53 and 54, each of which depends from allowable claim 52, are likewise allowable over the cited prior art.

Conclusion

For all of the above reasons, it is respectfully submitted that the claims now pending patentably distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

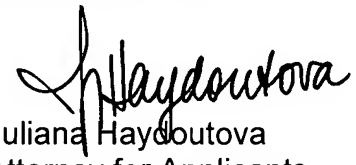
Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicant hereby petitions for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with

this communication to Deposit Account No. 01-2300, referring to client-matter number 108397-00106.

Respectfully submitted,

Arent Fox PLLC



Juliana Haydoutova
Attorney for Applicants
Registration No. 43,313

Customer No. 004372
1050 Connecticut Ave., N.W.
Suite 400
Washington, D.C. 20036-5339
Telephone No. (202) 715-8469
Facsimile No. (202) 638-4810

JH:ksm

TECH/281866.1